

AMENDMENTS TO THE CLAIMS

1. (Previously Presented) A transistor comprising:  
a first region of a first conductivity type;  
a second region of a second conductivity type that lies over the first region;  
a third region of the first conductivity type that contacts the second region,  
the third region being spaced apart from the first region; and  
a fourth region of the second conductivity type that contacts the third region,  
the fourth region being spaced apart from the second region.
2. (Previously Presented) The transistor of claim 1 and further comprising:  
a trench that extends from a top surface of the fourth region through the  
fourth region, the third region, and partially into the second region;  
a layer of insulation material that contacts the trench; and  
a conductive gate region that contacts the layer of insulation material and fills  
the trench.
3. (Original) The transistor of claim 2 wherein the conductive gate  
region is a region of doped polysilicon.
4. (Original) The transistor of claim 2 wherein the first, second, third,  
and fourth regions have a <110> crystallographic orientation.

5. (Original) The transistor of claim 2 and further comprising a plug that is formed through the first region to contact the second region.

6. (Original) The transistor of claim 5 wherein the plug is metallic.

7. (Original) The transistor of claim 5 and further comprising:  
a layer of isolation material that contacts the top surface of the fourth region, the layer of insulation material, and the conductive gate region;  
a gate contact formed through the layer of isolation material to make an electrical connection with the conductive gate region; and  
a drain contact formed through the layer of isolation material to make an electrical connection with the fourth region.

8. (Previously Presented) The transistor of claim 2 and further comprising an isolation layer that contacts the first and second regions.

9. (Previously Presented) The transistor of claim 1 and further comprising:  
a plurality of trenches that extend from a top surface of the fourth region through the fourth region, the third region, and partially into the second region;  
a plurality of insulation layers that contact the plurality of trenches such that each trench has an insulation layer; and  
a plurality of conductive gate regions that contact the plurality of insulation layers and fill up the trenches.

10. (Original) The transistor of claim 9 wherein the plurality of conductive gate regions are regions of doped polysilicon.
11. (Original) The transistor of claim 9 wherein the first, second, third, and fourth regions have a <110> crystallographic orientation.
12. (Original) The transistor of claim 9 and further comprising a plug that is formed through the first region to contact the second region.
13. (Original) The transistor of claim 10 wherein the plug is metallic.
14. (Original) The transistor of claim 10 and further comprising:  
a layer of isolation material that contacts the top surface of the fourth region, the plurality of insulation layers, and the plurality of conductive gate regions;  
a plurality of gate contacts formed through the layer of isolation material to make electrical connections with the conductive gate regions; and  
a plurality of drain contacts formed through the layer of isolation material to make electrical connections with the fourth region.
15. (Previously Presented) The transistor of claim 9 and further comprising an isolation layer that contacts the first and second regions.

Claims 16-24 (Cancelled)

25. (Previously Presented) The transistor of claim 8 wherein the isolation layer lies between the first and second regions, and is spaced apart from the layer of insulation material, the third region, and the fourth region.

26. (Previously Presented) The transistor of claim 15 wherein the isolation layer lies between the first and second regions, and is spaced apart from the plurality of insulation layers, the third region, and the fourth region.

27. (Previously Presented) The transistor of claim 12 wherein the plug is conductive and lies below two or more of the plurality of trenches.

28. (New) The transistor of claim 5 wherein the plug is conductive and spaced apart from the layer of insulation material.

29. (New) The transistor of claim 12 wherein the plug is conductive and spaced apart from each insulation layer.